REMARKS

By this Amendment, Claims 20-50 are pending, with Claim 20 as the only independent claim. Applicant believes all pending claims are now in condition for allowance which is respectfully requested.

1. Objection to Oath/Declaration

The Examiner states that the oath or declaration is defective. Applicant respectfully disagrees. As advised by the Examiner, consultation has been made to MPEP §601.01(a) which states:

> *The following combinations of information supplied in an oath or declaration filed on the application filing date with a specification are acceptable as minimums for identifying a specification and compliance with any one of the items below will be accepted as complying with identification requirement of 37 CFR 1.63:*
>
> *(A) name of inventor(s), and reference to an attached specification which is both attached to the oath or declaration at the time of execution and submitted with the oath or declaration on filing;*
>
> *(B) name of inventor(s), and attorney docket number which was on the specification as filed; or*
>
> *(C) name of inventor(s), and title which was on the specification as filed.*

In accordance with the above requirements, standard USPTO form PTO-FB-235 (French Language Declaration) was received by the Patent Office on February 26, 1999, appropriately identifying the name of the inventor and reference to an

attached specification filed therewith. Also, the name of the inventor and title to which was on the specification as filed was appropriately identified on the Declaration. Applicant has met and exceeded the minimum requirements of 37 CFR §1.63 by meeting more than one of the above identification requirements. Applicant respectfully requests correction of the record.

2. Objection to Specification

Applicant fails to understand the objection to the title, which is aptly descriptive of the invention. Reconsideration and withdrawal of this objection is respectfully requested.

3. Claim Objections

In the Office Action, the Examiner objects to Claim 20 for informalities. Claim 20 has been amended to more clearly recite the features of the invention. Still, the Examiner states that the language of Claim 20 is unclear because it implies both that there is a working memory associated with each program and not accessible by other programs and that each working memory is used by all programs. However, the Applicant asserts that there is no conflicting language in the claim as written, and therefore it is unnecessary to add a limiting feature without prior art to that effect. The Examiner also objects to Claims 20-50 for having reference numerals that imply that the specific type of device illustrated by the reference numerals will be used. Applicant has attended to removing the reference numerals so that the claims are not limited to the specific types of devices illustrated.

4. Rejection under 35 U.S.C. § 112

The Examiner rejects Claim 24 under 35 U.S.C. §112 for insufficient antecedent basis, stating it is unclear which working memory is being referred to. Claim 24 has been amended to recite a "first working memory."

5. Rejections under 35 U.S.C. § 103

Firstly, it may be beneficial to review some significant features of the present invention. Most pertinent to this Amendment is the feature of two working memories used in such a way as to make more difficult the detection of the execution of a secondary program. As taught in the prior art, a microprocessor containing only one working memory would facilitate easy observation of a secondary routine by observing the single working memory, respective of whether or not switching between processes is taught. By using two working memories, it makes it more difficult for a fraudulent person to determine which working memory is used and by which program, a main program or a secondary program. A further improvement of the invention is to combine the use of two working memories with the random running of a program by using either a random number generator, an interrupt circuit, or a time counting system controlling switching between the working memories. (Application, page 11, line 13, to page 12, line 12).

The Examiner rejects claims 20, 21, 23, 24, 27-36, 40, 41 and 50 as being unpatentable over Okin, U.S. Patent No. 5,361,337 (hereinafter referred to as "Okin") in view of Fletcher et al., U.S. Patent No. 5,012,409 (hereinafter referred to as "Fletcher"). Applicant respectfully traverses said rejection.

Okin discloses a method and apparatus of switching the context of state elements of a very fast processor within a clock cycle when a cache miss occurs. The object of such an invention is to increase processing efficiency (Okin, col. 2, lines 24-36).

The Examiner asserts that Okin discloses all elements of Claim 20 except an operating system for which Fletcher is relied on.

Okin's disclosure is not relevant to the art of the present invention. In contrast to Okin, the present invention teaches an unpredictable microprocessor comprising a switching means for switching, at random interrupts, between two working memories. Okin discloses a processor switching between processes, and not a processor switching between memories as is taught by the Applicant. Neither Okin nor Fletcher teaches or suggests the feature of "switching means for switching, while the programs are running, from one of the two working memories to the other working memory, while saving the contents of the two working memories" as recited in Claim 20. Therefore, the combination of Okin and Fletcher do not teach each and every element of the claimed invention.

Assuming arguendo that the Okin-Fletcher combination did teach every element of the claimed invention, the combination should not be applied to the art of the present invention because the functions performed by the elements are different from that of the invention. Thus, the combination does not suggest the claimed invention. The object of the Okin apparatus is to improve processor efficiency, while the object of the present invention is to improve processor security. The apparatus described by Okin is not adapted to accommodate an unpredictable processor as taught by the Applicant. Okin discloses an apparatus which cannot be used for the purposes of the present invention.

Fletcher discloses an Operating System (OS), and more particularly a multitasking operating environment for a multiplexer / demultiplexer application (Fletcher, col. 1, l. 6-9). Fletcher does not teach technical features for cooperation between an unpredicatable processor and an operating system since the disclosure does not teach particular switching means in order to use a first working memory or alternatively a second working memory. As with Okin, Fletcher teaches away from

the present invention. Fletcher does not disclose any feature to improve security in a processor.

While one may make the Okin-Fletcher combination to arrive at an apparatus for process coordination, it is not reasonable to assert that one of ordinary skill in the art would make the Okin-Fletcher combination to arrive at the present invention, nor expect to achieve the result of the claimed combination.

Referring to claim 23, Okin does not disclose that the main program can enable or inhibit the switching mechanism or mechanisms by loading the switching circuit for switching and enabling the working memories and blocks of storage registers associated with each respective working memory, and storing, respectively, the operating context of the programs in the main memory and the operating context of the secondary program. The Examiner asserts it would have been obvious to a person skilled in the art to incorporate the main program of Fletcher, because a main program is needed to control the processor's function. However, Claim 23 clearly states that the main program controls the switching mechanism, and not necessarily a processor. Fletcher teaches no such main program. Furthermore, Okin teaches an apparatus for switching the context of state elements in a very fast processor upon occurrence of a cache miss. Accordingly, the main program of Okin is different and not adapted to control a switching mechanism concerning a first and a second working memory so as to obtain an unpredictable processor.

Even if the features of Claims 21, 23, 24, 27-36, 40, 41, and 50 is considered not new or obvious by the Examiner, at least by virtue of its dependency from Claim 20, the combination of features claimed is new and non-obvious.

The Examiner rejects Claims 22, 25, 26, 37, 39, 42-49 as being unpatentable over Okin in view of Fletcher, and further in view of Griffin III et al. U.S. Patent No.

5,249,294 (hereinafter referred to as "Griffin"). Applicant respectfully traverses said rejection.

The Griffin disclosure is directed to preventing compromise of a secure data processing routine by a procedure known as a "clock attack" (Griffen col. 1, l. 12-14). Griffen discloses the step of randomly varying the duration between occurrence of an externally observable event and the execution of a predetermined routine. This purpose is disconnected from the purpose of Okin, which is directed to processing efficiency. This purpose is also disconnected from the purpose of Fletcher, which is directed to an operating system for a multi-tasking operating environment. Furthermore, the processing method (Griffin, col. 3, l. 11-63) according to Griffin is completely different from the processing method according to the invention. Applicant believes the Examiner relies on improper "pick and choose" for attempting to reach the claimed invention, but there is no suggestion to combine these references or that the references can be so combined to produce the result of the claimed combinations.

Referring to Claim 26, Okin does not teach that the de-correlating means comprise a time counting system independent from the processor for, after the time count, triggering an interrupt for returning from the secondary program to the main program. Okin does not teach this feature because the apparatus according to Okin is adapted to rapidly switching processes in a computer system when a cache miss occurs.

Referring to claim 39, Okin does not disclose means of de-correlating the run-through of the programs with respect to an isochronal clock.

Even if the features of Claims 22, 25, 26, 37, 39, 42-49 is considered not new or obvious by the Examiner, at least by virtue of its dependency from Claim 20, the combination of features claimed is new and non-obvious.

The Examiner asserts that claim 38 is unpatentable over Okin in view of Fletcher and further in view of Takagi, U.S. Patent No. 5,280,618 (hereinafter referred to as "Takagi"). Applicant respectfully traverses said rejection.

The Takagi disclosure is directed to an interrupt test circuit for a digital processor which facilitates interrupt performance tests. Takagi does not disclose any feature to improve security in a processor. Again, there is no suggestion to combine the references.

Even if the feature of Claim 38 is considered not new or obvious by the Examiner, at least by virtue of its dependency from Claim 20 the combination of features claimed is new and non-obvious.

Inasmuch as the combination of Okin and Fletcher do not teach or suggest the present invention, Applicant respectfully submits Claim 20 and all claims dependent thereon are neither anticipated nor rendered obvious in view of Okin and Fletcher.

Applicant respectfully requests reconsideration of the application and withdrawal of the rejection of all pending claims in view of the foregoing arguments. All pending claims are believed to be in condition for allowance and passage of the application to issue at an early date is earnestly solicited.

The Commissioner is hereby authorized to charge to deposit account number 50-1165 and fees not included herein, under 37 CFR §§ 1.16 and 1.17, that may be required by this paper and to credit any overpayment to that Account. A duplicate copy of this page is included for such purpose. If any additional extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

MILES & STOCKBRIDGE P.C.

3/20/03

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